

**IN THE CLAIMS:**

Claims 1-9 (Cancelled)

10. (Original) A method of fabricating a silicon-on-insulator (SOI) metal oxide field effect transistor (MOSFET) device comprising the steps of:

providing a structure including at least a back-gate oxide located atop a Si-containing layer, said Si-containing layer is a component of a SOI wafer;

forming alternating regions of back-gate-STI and first polysilicon atop said back-gate oxide;

forming a second polysilicon layer atop said alternating regions of back-gate-STI and first polysilicon;

implanting a back-gate region into said polysilicon layers;

forming an oxide layer on said second polysilicon layer;

bonding a holding-substrate wafer to said oxide layer and flipping the bonded structure to expose layers of said SOI wafer;

removing selective layers of said SOI wafer stopping on said Si-containing layer;

converting a portion of said Si-containing layer into a body region; and

forming a gate dielectric and a polysilicon gate atop said body region.

11. (Original) The method of Claim 10 further comprising forming raised source/drain regions atop said body region that lays adjacent to said polysilicon gate.

12. (Original) The method of Claim 11 further comprising converting said raised source/drain regions into silicide regions.

13. (Original) The method of Claim 10 wherein said bonding is performed at a temperature of about 900°C to about 1100°C for a time period of from about 1.5 hours to about 2.5 hours.

14. (Original) The method of Claim 10 wherein said bonding is performed at a temperature of from about 18°C to about 27°C in an inert ambient.

15. (Original) The method of Claim 10 wherein said body region is formed by a masked ion implantation process.

16. (Original) The method of Claim 10 wherein said alternating polysilicon region have under-cut sidewalls.

17. (Original) The method of Claim 10 further comprising encapsulating said polysilicon gate with a dielectric material, said dielectric material having conductively filled contact holes abutting said polysilicon gate.